

MMUB65R115RU(P)RH

650V 0.115Ω N-channel MOSFET

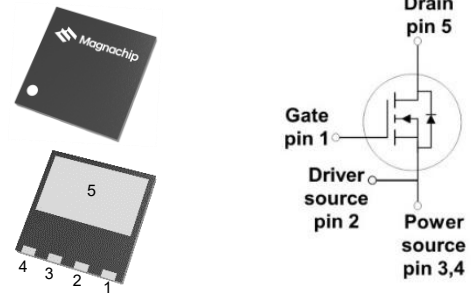
■ Description

MMUB65R115RU(P) is power MOSFET using Magnachip's advanced super junction technology that can realize very low on-resistance and gate charge. It will provide much high efficiency by using optimized charge coupling technology. These user friendly devices give an advantage of Low EMI and low switching loss as well as excellent ESD capability to designers.

■ Key Parameters

| Parameter | Value | Unit |
|----------------------|-------|------|
| $V_{DS} @ T_{j,max}$ | 700 | V |
| $R_{DS(on),max}$ | 0.115 | Ω |
| $V_{GS(th),typ}$ | 3.0 | V |
| I_D | 30 | A |
| $Q_{g,typ}$ | 64.0 | nC |

■ Package & Internal Circuit



■ Features

- Low Power Loss by High Speed Switching and Low On-Resistance
- Excellent ESD robustness
- 100% Avalanche Tested
- Green Package – Pb Free Plating, Halogen Free

■ Applications

- Premium OLED TV
- PFC Power Supply Stages
- Switching Applications
- Adapter

■ Ordering Information

| Order Code | Marking | Temp. Range | Package | Packing | RoHS Status |
|------------------------------|---------|--------------|---------|---------|-------------|
| MMUB65R115RURH | 65R115R | -55 ~ 150 °C | PDFN88 | Reel | Compliant |
| MMUB65R115RPRH ¹⁾ | 65R115R | -55 ~ 150 °C | PDFN88 | Reel | Compliant |

1) MMUB65R115RPRH : Pure Pb free solder wire

■ Absolute Maximum Rating ($T_c=25\text{ }^\circ\text{C}$ unless otherwise specified)

| Parameter | Symbol | Rating | Unit | Note |
|---|-----------|----------|------------------|---------------------------------|
| Drain – Source voltage | V_{DSS} | 650 | V | |
| Gate – Source voltage | V_{GSS} | ± 30 | V | |
| Continuous drain current ²⁾ | I_D | 30 | A | $T_C=25\text{ }^\circ\text{C}$ |
| | | 19 | A | $T_C=100\text{ }^\circ\text{C}$ |
| Pulsed drain current ³⁾ | I_{DM} | 90 | A | |
| Power dissipation | P_D | 260 | W | |
| Single - pulse avalanche energy ⁴⁾ | E_{AS} | 740 | mJ | |
| MOSFET dv/dt ruggedness | dv/dt | 50 | V/ns | |
| Diode dv/dt ruggedness ⁵⁾ | dv/dt | 50 | V/ns | |
| Storage temperature | T_{stg} | -55 ~150 | $^\circ\text{C}$ | |
| Maximum operating junction temperature | T_j | 150 | $^\circ\text{C}$ | |

2) I_D limited by maximum junction temperature

3) Pulse width t_P limited by $T_{j,max}$

4) $I_{AS} : 9\text{ A}$

5) $I_{SD} \leq I_D$, $V_{DS\ peak} \leq 400\text{V}$, $T_j=25\text{ }^\circ\text{C}$

■ Thermal Characteristics

| Parameter | Symbol | Value | Unit |
|--|------------|-------|--------------------|
| Thermal resistance, junction-case max | R_{thjc} | 0.48 | $^\circ\text{C/W}$ |
| Thermal resistance, junction-ambient max | R_{thja} | 62.5 | $^\circ\text{C/W}$ |

■ Static Characteristics ($T_c=25\text{ }^\circ\text{C}$ unless otherwise specified)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Condition |
|----------------------------------|---------------|------|-------|-------|----------|-----------------------------------|
| Drain – Source breakdown voltage | $V_{(BR)DSS}$ | 650 | - | - | V | $V_{GS} = 0V, I_D = 1mA$ |
| Gate threshold voltage | $V_{GS(th)}$ | 2.0 | 3.0 | 4.0 | V | $V_{DS} = V_{GS}, I_D = 250\mu A$ |
| Zero gate voltage drain current | I_{DSS} | - | - | 1 | μA | $V_{DS} = 650V, V_{GS} = 0V$ |
| Gate leakage current | I_{GSS} | - | - | 100 | nA | $V_{GS} = \pm 30V, V_{DS} = 0V$ |
| Drain-Source on state resistance | $R_{DS(ON)}$ | - | 0.102 | 0.115 | Ω | $V_{GS} = 10V, I_D = 15A$ |

■ Dynamic Characteristics ($T_c=25\text{ }^\circ\text{C}$ unless otherwise specified)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Condition |
|---|--------------|------|------|------|----------|--|
| Input capacitance | C_{iss} | - | 2292 | - | pF | $V_{DS} = 400V, V_{GS} = 0V, f = 400kHz$ |
| Output capacitance | C_{oss} | - | 57 | - | | |
| Reverse transfer capacitance | C_{rss} | - | 9.0 | - | | |
| Effective output capacitance energy related ⁶⁾ | $C_{o(er)}$ | - | 101 | - | | |
| Turn on delay time | $t_{d(on)}$ | - | 37 | - | ns | $V_{GS}=10V, R_G=25\Omega, V_{DD}=325V, I_D=30A$ |
| Rise time | t_r | - | 62 | - | | |
| Turn off delay time | $t_{d(off)}$ | - | 206 | - | | |
| Fall time | t_f | - | 47 | - | | |
| Total gate charge | Q_g | - | 64.0 | - | nC | $V_{GS}=10V, V_{DD}=520V, I_D=30A$ |
| Gate – Source charge | Q_{gs} | - | 12.0 | - | | |
| Gate – Drain charge | Q_{gd} | - | 30.6 | - | | |
| Gate resistance | R_G | - | 4.9 | - | Ω | $V_{GS} = 0V, f = 1.0MHz$ |

6) $C_{o(er)}$ is a capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0V to 80% $V_{(BR)DSS}$

■ Reverse Diode Characteristics ($T_c=25^\circ\text{C}$ unless otherwise specified)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Condition |
|----------------------------------|-----------|------|------|------|---------------|--|
| Continuous diode forward current | I_{SD} | - | - | 30 | A | |
| Diode forward voltage | V_{SD} | - | - | 1.4 | V | $I_{SD} = 30\text{A}$, $V_{GS} = 0\text{V}$ |
| Reverse recovery time | t_{rr} | - | 516 | - | ns | $I_{SD} = 30\text{A}$ $di/dt = 100\text{A}/\mu\text{s}$ $V_{DD} = 100\text{V}$ |
| Reverse recovery charge | Q_{rr} | - | 9.9 | - | μC | |
| Reverse recovery current | I_{rrm} | - | 38.5 | - | A | |

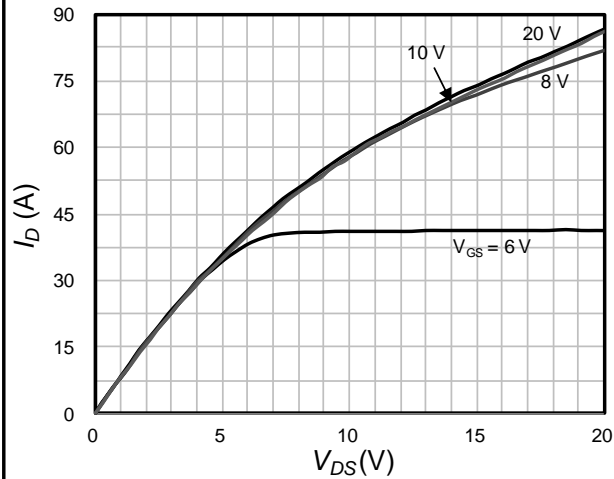
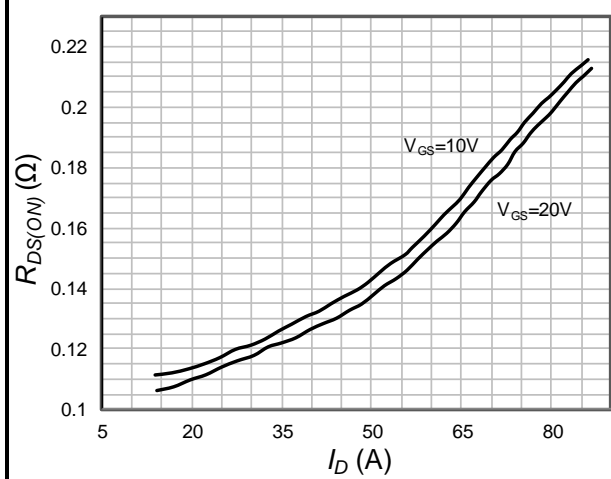
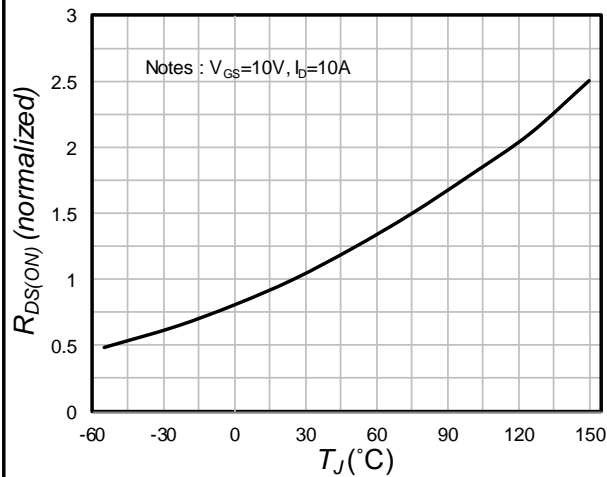
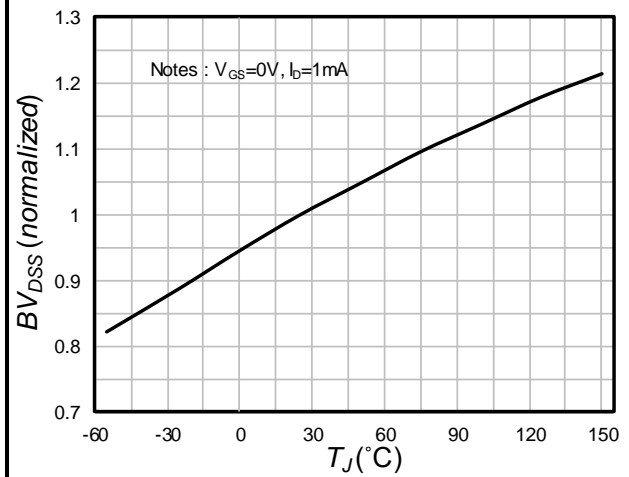
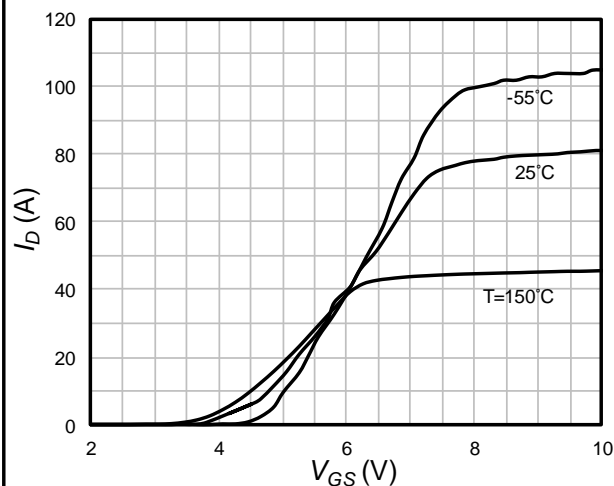
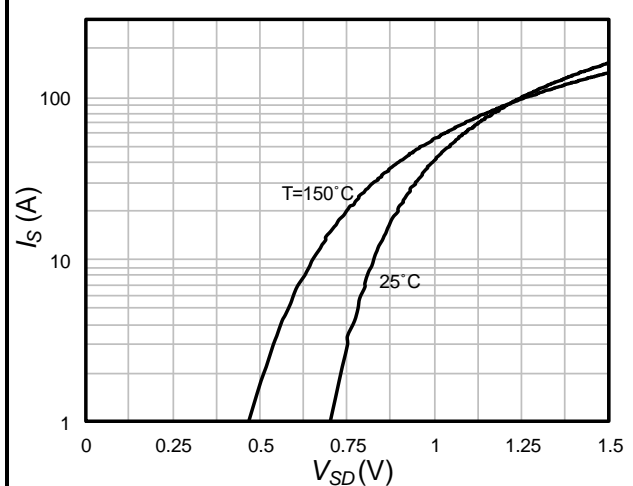
■ Characteristic Graph
Fig.1 On-Region characteristics.

Fig.2 On-resistance variation with drain current

Fig.3 On-resistance variation with junction temperature (normalized)

Fig.4 Breakdown voltage variation with temperature (normalized)

Fig.5 Transfer characteristics

Fig.6 Diode forward characteristics


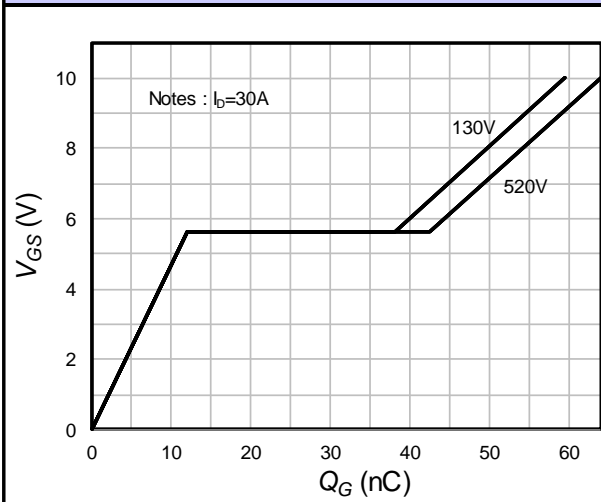
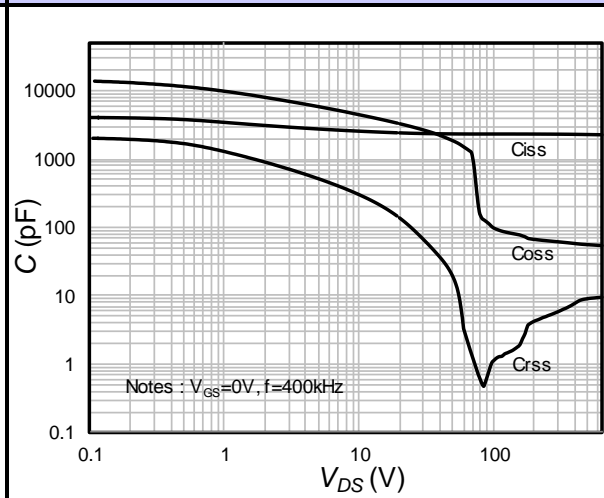
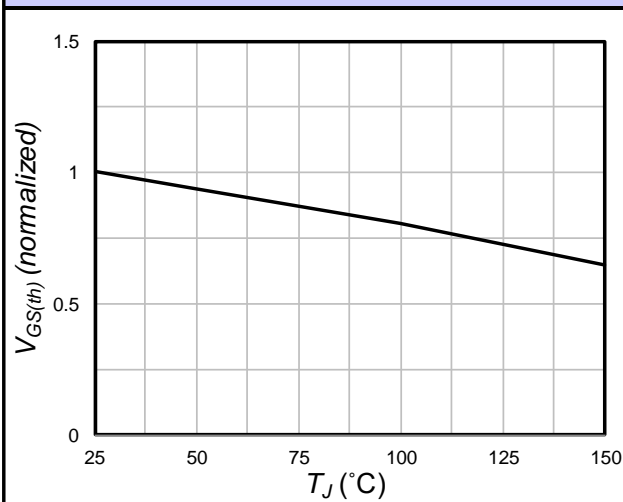
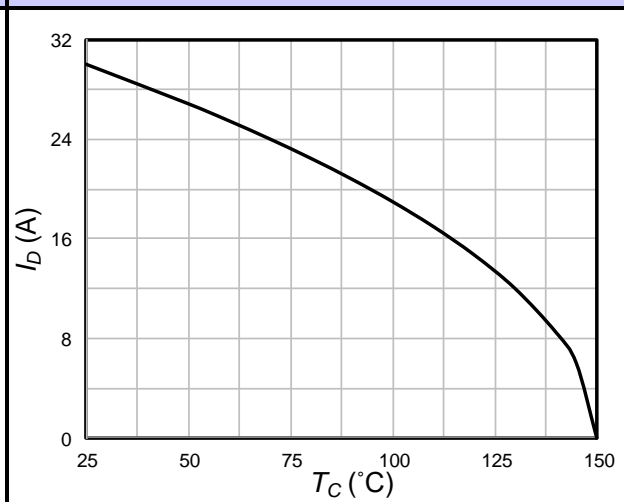
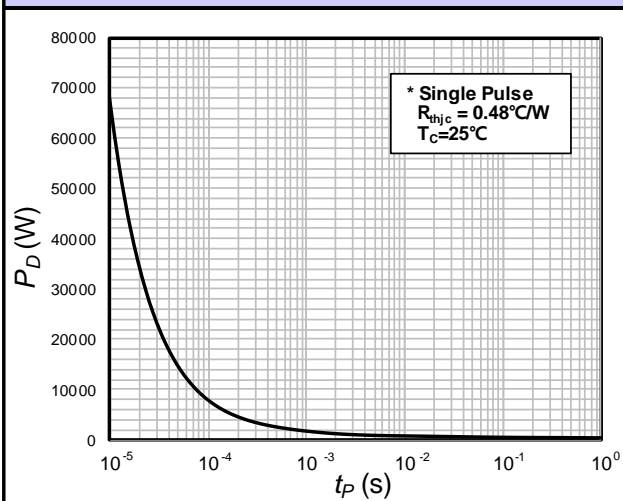
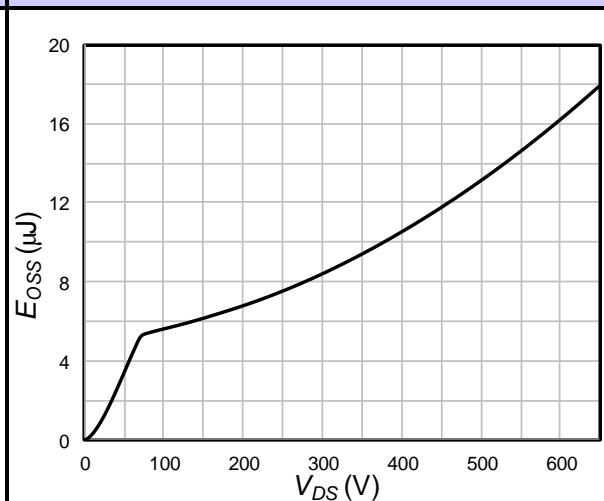
Fig.7 Gate charge characteristics

Fig.8 Capacitance characteristics

Fig.9 Threshold voltage variation with junction temperature

Fig.10 Drain current

Fig.11 power dissipation variation with pulse time

Fig.12 Output capacitance stored energy


Fig.13 Transient thermal response

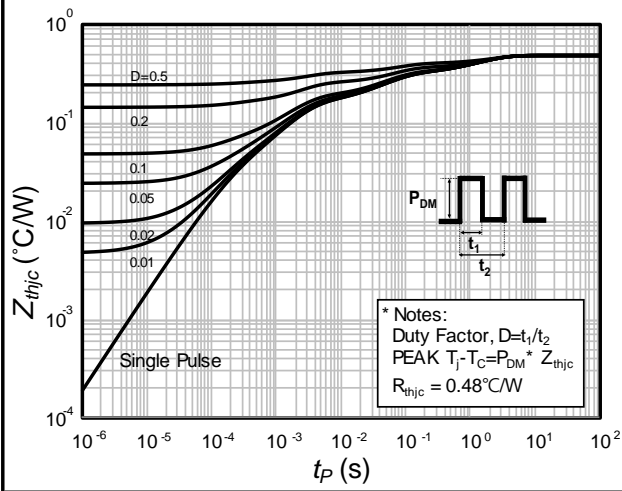
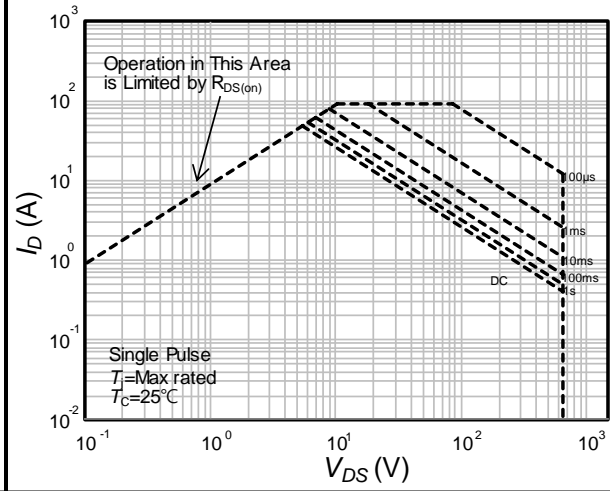


Fig.14 Safe operating area



■ Test Circuit

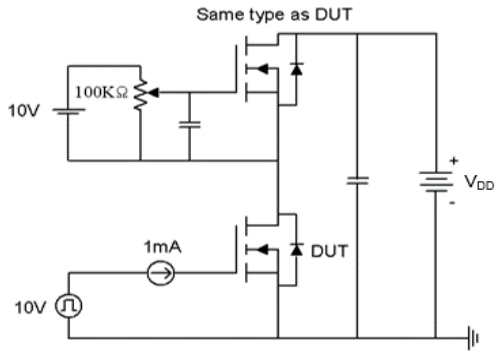


Fig15-1. Gate charge measurement circuit

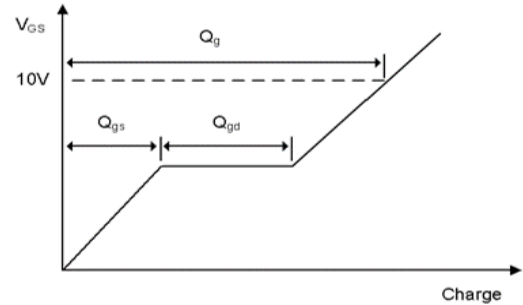


Fig15-2. Gate charge waveform

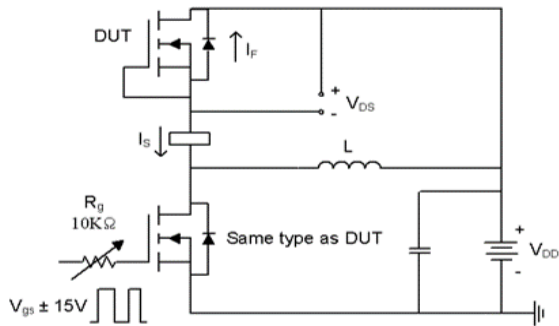


Fig16-1. Diode reverse recovery test circuit

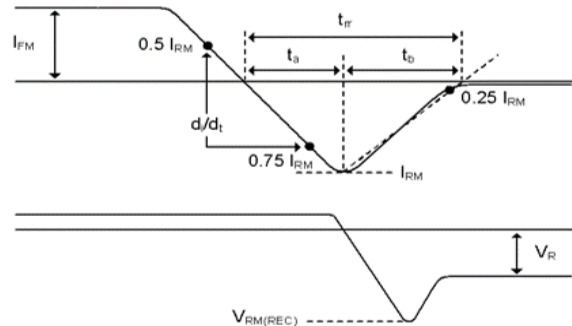


Fig16-2. Diode reverse recovery test waveform

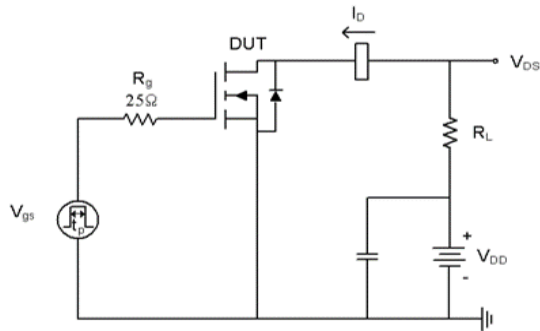


Fig17-1. Switching time test circuit for resistive load

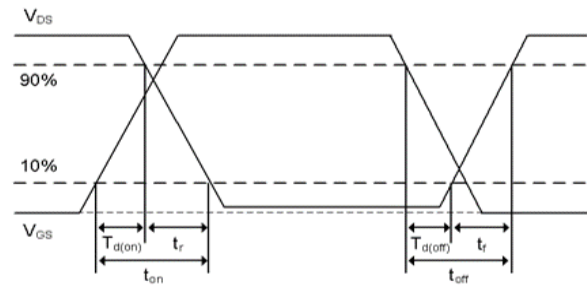


Fig17-2. Switching time waveform

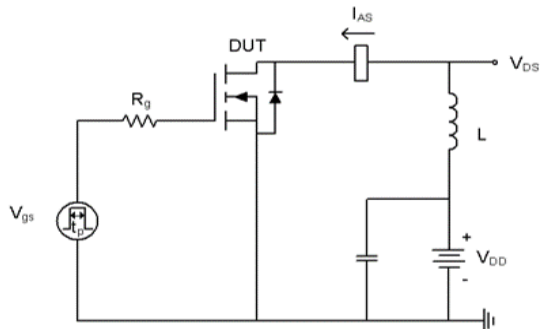


Fig18-1. Unclamped inductive load test circuit

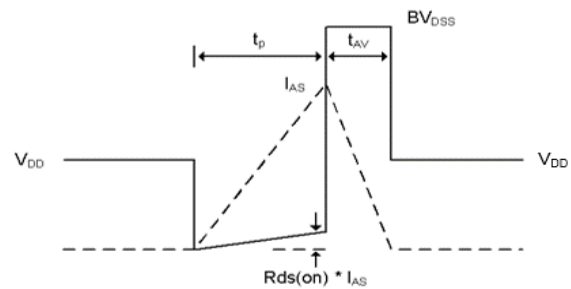
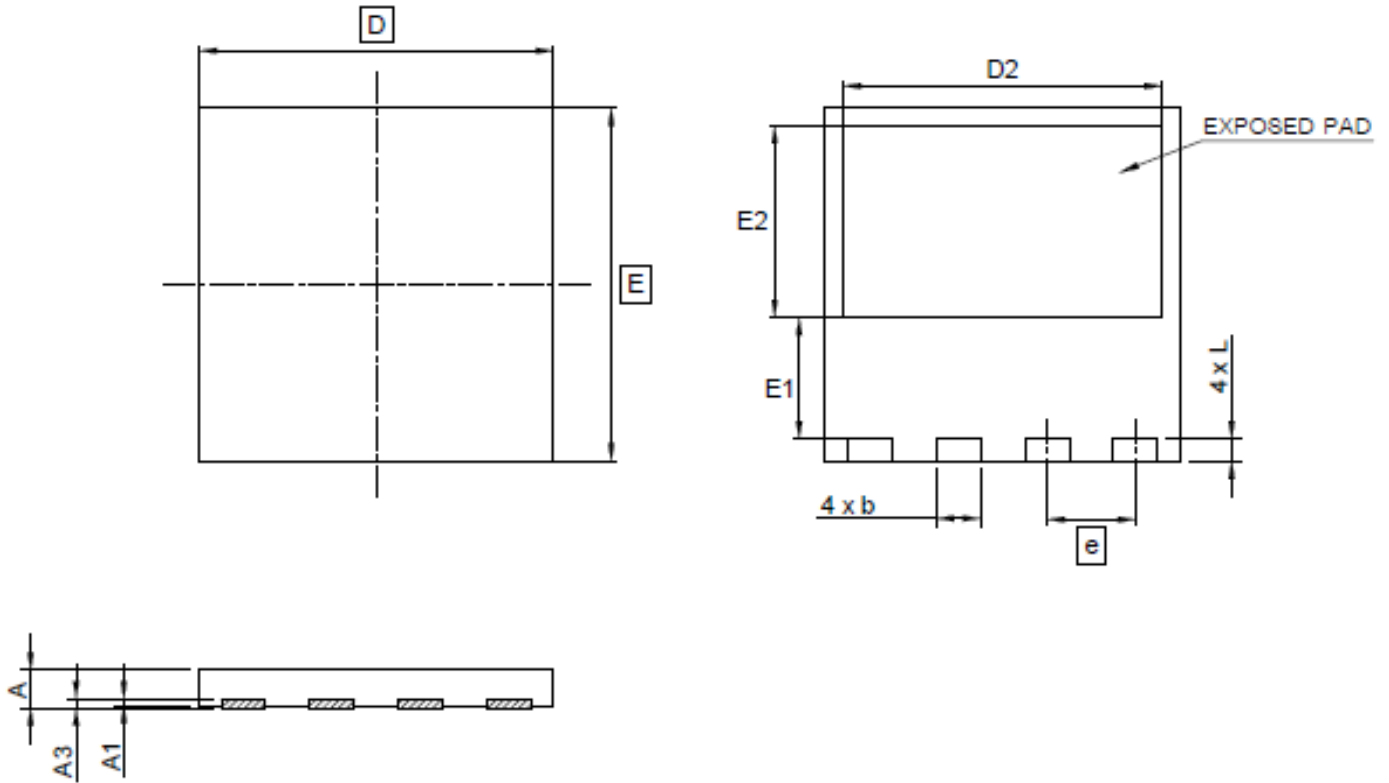


Fig18-2. Unclamped inductive waveform


Physical Dimension
PDFN88


Note : Package body size, length and width do not include mold flash, protrusions and gate burrs

| Symbol | Dimension (mm) | | |
|--------|----------------|------|------|
| | Min | Nom | Max |
| A | 0.75 | 0.85 | 0.95 |
| A1 | 0.00 | - | 0.05 |
| A3 | 0.10 | 0.20 | 0.30 |
| b | 0.90 | 1.00 | 1.10 |
| D | 7.90 | 8.00 | 8.10 |
| E | 7.90 | 8.00 | 8.10 |
| D2 | 7.10 | 7.20 | 7.30 |
| E1 | 2.65 | 2.75 | 2.85 |
| E2 | 4.25 | 4.35 | 4.45 |
| e | 2.00 B9C | | |
| L | 0.40 | 0.50 | 0.60 |

DISCLAIMER:

The Products are not designed for use in hostile environments, including, without limitation, aircraft, nuclear power generation, medical appliances, and devices or systems in which malfunction of any Product can reasonably be expected to result in a personal injury. Seller's customers using or selling Seller's products for use in such applications do so at their own risk and agree to fully defend and indemnify Seller.

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